REMARKS/ARGUMENTS

This Amendment is filed in response to the Office Action mailed on September 7, 2006. Claims 1, 2, 3, 4, 5, 7, 8, 9, 10, 11, 13, 14, 15, 16, 18, 20, 21, 22, 28, 29, and 31 are amended. Claims 24-28, and 30 are cancelled. New claims 32-34 are presented.

Priority

Applicants submit herewith the certified copies of Japanese application numbers 2003-050243 and 2003-028998 as required by 35 U.S.C. §119(b).

Specification

Applicants have amended the title of the invention as suggested by the Examiner.

Section 112 Issues

The Office Action rejected claims 1-8 under 35 USC §112 due to lack of antecedent basis in claim 1 for "said host." This typographical error has been corrected to now read "a host".

Section 102 Issues

The Office Action initially rejected claims 1-31 as being anticipated by Hoshino (US 6,003,113). Claims 1, 2, 3, 4, 5, 7, 8, 9, 10, 11, 13, 14, 15, 16, 18, 20, 21, 22, 28, 29, and 31 have been amended to more clearly recite the claimed invention. In addition, new claims 32-34 have been presented. Finally, to focus the issues under review, claims 24-28, and 30 have been cancelled.

In regard to claim 1, the claim now recites the claim element "wherein said IC chip, said nonvolatile memory and said controller are comprised of separate chips." The Hoshino reference in contrast teaches that its area control mechanism 5 and memory area are inside its portable card 1 (see Fig. 1 of Hoshino) -- i.e., Hoshino's controller and nonvolatile

memory are inside the IC chip. Thus, Hoshino does not teach that the IC chip, the nonvolatile memory, and the controller are comprised of separate chips.

In addition, claim 1 and subsequent claims have been amended to more clearly recite that the memory is a nonvolatile memory.

In regard to claim 3, the Office Action indicated that Fig. 4 of Hoshino illustrates the claim element added by claim 3. However, claim 3 now includes the limitation of "through said controller". The Hoshino reference does not teach "an operation code used to transfer said associated data associated with said one application program between said nonvolatile memory and said IC chip through said controller".

In regard to claim 5, Hoshino appears to teach that a host processor transfers an application ID. However, claim 5 has been clarified by amendment to recite that the IC chip transfers the application ID. Therefore, Hoshino does not teach that "said IC chip transfers an application ID in said IC chip" as recited in claim 5.

Claim 9 is in condition for allowance for the same reason as claim 1. Namely, claim 9 recites that the IC chip, the nonvolatile memory and the controller are separate chips. Furthermore, as noted above, Hoshino does not teach that the IC chip issues the operation execution instruction; rather, in Hoshino, the host processor appears to issue the operation execution instruction.

In regard to claim 10, the Hoshino reference does not teach any command for transferring data between the portable card 1 and memory area 2 through the control mechanism 5 of Hoshino. Therefore, Hoshino does not teach the element of claim 10 that recites "wherein said command code includes a first transfer command for transferring data to be written to a block in said nonvolatile memory from said IC chip to said controller and a second transfer command for transferring data read from a block in said nonvolatile memory by said controller to said IC chip. For at least this additional reason, claim 10 is allowable.

As to claim 13, the Hoshino reference again does not teach that the IC chip, the nonvolatile memory, and the controller are comprised of separate chips. Thus, claim 13 is allowable for the same reason that claim 1 is allowable.

In regard to claim 22, the Hoshino reference does not teach any command for transferring data between the portable card 1 and memory area 2 through the control mechanism 5 of Hoshino. Thus, the Hoshino reference does not teach "transfer command codes for identifying transfer commands for receiving data read from said second area of said nonvolatile memory from said IC chip and for sending data to be written to said second area to said IC chip". Furthermore, Hoshino also does not teach that its area control mechanism generates a transfer command. Hoshino therefore does not teach "wherein said controller generates, for each application program, transfer command codes." For at least these additional reasons, claim 22 is allowable.

In regard to claim 28, the Office Action asserts that Fig. 5 of Hoshino illustrates the limitation cited in claim 28. However, while Hoshino illustrates a space table for controlling the area, Hoshino does not illustrate the format of transfer data between the controller and the IC chip. Therefore, Hoshino does not teach that "said IC chip sends to said controller output data including a first control byte, a second control byte, and trailing output data according to format of the ISO 7816 specifications."

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

William F. Vobach
Reg. No. 39,411

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 303-571-4000
Fax: 415-576-0300

WFV:klb
60916205 v1